REMARKS

Claims 1, 3-10, and 12-19 are pending. The Examiner's reconsideration of the objections and rejections is respectfully requested in view of the amendments and remarks.

The Examiner has objected to the drawings; specifically, Figure 13 as including two labels 1303, and Figures 3(A)-3(C) as including illegible labels and small features. Proposed drawing corrections for Figure 13 and Figures 3a-3c are attached hereto. In Figure 13 the first label 1303 has been amended to 1301. The labels of Figures 3a-3c have been enlarged and features of the Figures clarified. The Examiner's reconsideration of the objections in view of the proposed drawing corrections is respectfully requested.

The Examiner has objected to the specification for various informalities.

Applicants appreciate the Examiner's suggestions within respect to the informalities listed under section 2.1 of the Office Action. Referring to the Examiner's suggestion that page 11 lines 1-8 is unclear, Applicants point to Figures 3(A)-3(C) and Figure 5 to show how the "AND" function performs. At a given bit, all addresses must fail to determine a fail, see for example, page 13, lines 6-10. The Examiner's suggestions with respect to the other objections in section 2.1 are believed to be reflected in the amendments to the specification above. The Examiner's reconsideration of the objection is respectfully requested.

Referring to the Examiner's objection of the specification as not sufficiently describing or explaining "holding an address at a potential", the Examiner has indicated that the phrase is being read as holding an address at a specific value (i.e., 0 or 1). Respectfully, one of ordinary skill in the art would recognize that a potential can be assigned different labels, such as the labels suggested by the Examiner. The specification describes a first potential and a second potential. The specification also describes a state as high or low, e.g., 1 or 0, for example, at page 12, line

5. Therefore, the specification is believed to adequately describe the invention as claimed. The Examiner's reconsideration of the objection is respectfully requested.

Referring to the Examiner's objection of the specification as being contradictory, the different sentences cited by the Examiner reflect different, but overlapping, possibilities. The test pattern may be a single address and it may also be one or more addresses. Respectfully, Applicants believe that the sentences are not contradictory. Accordingly, the Examiner's reconsideration of the objection is respectfully requested.

Claims 1 and 10 have been objected to as including the term "addresses". The term has been amended to --address--. The Examiner's reconsideration of the objection is respectfully requested.

Claims 1-17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kalter et al. (U.S. Patent No. 5,961,653) in view of Schanstra et al., "Semiconductor Manufacturing Process Monitoring Using Built-In Self-Test For Embedded Memories" (hereinafter Schanstra). The Examiner stated essentially that the combined teachings of Kalter and Schanstra teach or suggest all of the limitations of claims 1-17.

Claims 1 and 10 claim, *inter alia*, "determining a fail string for the device including pass/fail results for the test pattern, wherein different subsets of the fail string correspond to different fail types."

Kalter teaches that failures are determined based on testing of a complete address space (see col. 8, lines 28-31). Kalter does not teach determining a fail string for the device including pass/fail results for the test pattern, wherein different subsets of the fail string correspond to different fail types as claimed in claims 1 and 10. The complete address space is not a fail strings as claimed in claims 1 and 10. Kalter teaches that different registers include failed data

bits and failed wordlines (see col. 9, line 57 to col. 10, line 14). Different failure types of Kalter are separated in different registers. The different fail types of Kalter are not found in a single fail string. Thus, Kalter does not teach a fail string, wherein different subsets of the fail string correspond to different fail types, essentially as claimed in claims 1 and 10. Therefore, Kalter fails to teach all the limitations of claims 1 and 10.

Schanstra teaches running a BIST testing in an entire memory (see page 875, first col., last paragraph). Schanstra does not teach or suggest "determining a fail string for the device including pass/fail results for the test pattern, wherein different subsets of the fail string correspond to different fail types" as claimed in claims 1 and 10. Schanstra teaches determining different fault types from a bitmap (see page 873, sections 2.1 and 2.2). The bitmap of Schanstra is not a fail string as claimed in claims 1 and 10. The bitmap of Schanstra is a two-dimensional rendering of memory failures. Thus, the bitmap is not a string, much less a fail string, wherein different subsets of the fail string correspond to different fail types as claimed in claims 1 and 10. Therefore, Schanstra fails to cure the deficiencies of Kalter.

The combined teachings of Kalter and Schanstra fail to teach or suggest "determining a fail string for the device including pass/fail results for the test pattern, wherein different subsets of the fail string correspond to different fail types" as claimed in claims 1 and 10.

Claims 3-9 depend from claim 1. Claims 12-17 depend from claim 10. The dependent claims are believed to be allowable for at least the reasons given for the independent claims, respectively.

At least claims 8 and 17 are believed to be allowable for additional reasons.

Claims 8 and 17 claim, *inter alia*, "determining the failing cell upon determining a fail in the pass/fail results for every x-y address combination addressing the failing cell; and

determining the passing cell upon determining any one passing x-y address combination addressing the passing cell."

Kalter teaches a BIST test for determining bit and wordline failures (see col. 8, lines 36-51). Kalter does not teach that "determining the passing cell upon determining any one passing x-y address combination addressing the passing cell" as claimed in claims 8 and 17. Kalter teaches that once a bit is determined to have failed, no other consideration is needed of that bit (see col. 9, line 57 to col. 10, line 14). Kalter does not teach determining the passing cell upon determining any one passing x-y address combination addressing the passing cell. Thus, Kalter does not teach all the limitations of claims 8 and 17.

Schanstra teaches running a BIST test in an entire memory (see page 875, col. 1, last paragraph). Schanstra does not teach or suggest "determining the passing cell upon determining any one passing x-y address combination addressing the passing cell" as claimed in claims 8 and 17. Schanstra teaches an uncompressed bitmap wherein, if at least one read operation on a certain memory cell has failed, the corresponding location is considered to fail (see page 873, section 2.1). Schanstra does not teach or suggest a pseudo compressed bitmap, wherein if any one x-y address combination which addresses the bit is determined to pass then the bit is determined to pass, essentially as claimed in claims 8 and 17. Therefore, Schanstra fails to cure the deficiencies of Kalter.

The combined teachings of Kalter and Schanstra fail to teach "determining the passing cell upon determining any one passing x-y address combination addressing the passing cell" as claimed in claims 8 and 17. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 18 and 19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Schanstra. The Examiner stated essentially that Schanstra teaches or suggests all the limitations of claim 18 and 19.

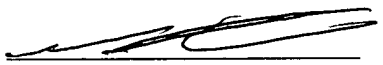
Claim 18 claims, *inter alia*, "generating a pseudo compressed bitmap by combining a plurality of pass/fail results of a fail string; and displaying the pseudo compressed bitmap wherein the pass/fail results correspond to at least one X address pin and one Y address pin, and wherein each address pin corresponds to a plurality of pass/fail results, wherein a bit is determined to pass in the pseudo compressed bitmap upon determining that any address pin that addresses the bit passes."

Schanstra teaches that if at least one read operation on a certain memory cell has failed, the corresponding location is considered to fail (see page 873, section 2.1). Schanstra does not teach or suggest that "wherein a bit is determined to pass in the pseudo compressed bitmap upon determining that any address pin that addresses the bit passes." Schanstra teaches a bit by bit determination of a bitmap, wherein a bit is determined to have failed upon determining one failure. Schanstra does not teach or suggest a pseudo compressed bitmap "wherein a bit is determined to pass in the pseudo compressed bitmap upon determining that any address pin that addresses the bit passes." Schanstra teaches that a failure is determinative of a bit's pass/fail value. Schanstra does not teach that a pass is determinative of a bit's pass/fail value. Accordingly, Schanstra fails to teach or suggest all the limitations of claim 18.

Claim 19 depends from claim 18. Claim 19 is believed to be allowable for at least the reasons given for claim 18. The Examiner's reconsideration of the rejection is respectfully requested.

Accordingly, claims 1, 3-10, and 12-19 are believed to be allowable for at least the reasons stated. The Examiner's reconsideration of the objections and rejections is respectfully requested. For the forgoing reasons, the application is believed to be in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

By: 

Nathaniel T. Wallace
Reg. No. 48,909
Attorney for Applicant(s)

Mailing Address:
F. Chau & Associates, LLC
1900 Hempstead Turnpike
Suite 501
East Meadow, NY 11554
(516) 357-0091
(516) 357-0092 (FAX)